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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,607	08/04/2003	Huajie Chen	FIS920030199US1	1606

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,607	CHEN ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) 13-29 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, drawn to an integrated circuit, classified in class 257, subclass 265.

II. Claims 13-29, drawn to a method of forming an integrated circuit, classified in class 438, subclass 199.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the product can be formed by materially different process, for example forming a silicon germanium by implant and sputter deposition.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Daniel Schnurmann on 6/29/04 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-12. Affirmation of this election must be made by applicant in replying to this Office

action. Claims 13-29 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Oath/Declaration

Oath/Declaration filed on 9/25/03 has been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Xiang et al. (U.S. Patent No. 6,703,648).

Referring to figures 3a-3i, Xiang et al. a teaches an integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) (see col. 7, lines 20-24) and an n-type field effect transistor (NFET) (see col. 7, lines 20-24) wherein a first strain is applied to the channel region of the PFET but not the NFET (see col. 7, lines 20-24), via a semiconductor layer disposed in source and drain regions of the PFET (see col. 3, lines 13-43) and not the NFET (see col. 7, lines 20-24), the semiconductor layer being lattice-mismatched to a single-crystal semiconductor disposed in the channel regions of the PFET and NFET (see col. 3, lines 13-43. Noted that silicon germanium or silicon (40) has a lattice-mismatched).

Regarding to claim 2, the channel regions of the PFET and the NFET are disposed in a single crystal region of the first semiconductor (40) and the lattice-mismatched semiconductor includes a layer of a second semiconductor (42) disposed over the single-crystal region of the first semiconductor (see figure 3a-3b, col. 3, lines 63+).

Regarding to claim 3, the single crystal region of the first semiconductor has a main surface defined by a level of a gate dielectric of a gate stack of the PFET (56/54/58, see figure 3c) and the layer of the second semiconductor has a top surface disposed beneath and main surface (40, see figure 3a-3f).

Regarding to claim 4, single-crystal layer of the first semiconductor (42) disposed over of the second semiconductor (40, see figure 10).

Regarding to claim 5, the first semiconductor consists essentially of a semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide (see figure 3a-3b, col. 3, lines 63+) and the second semiconductor consists essentially of another semiconductor different from the first semiconductor, the another semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide (see figure 3a-3b, col. 3, lines 63+).

Regarding to claim 6, the first semiconductor consists essentially of silicon and the second semiconductor consists essentially of silicon germanium (see figure 3a-3b, col. 3, lines 63+).

Regarding to claim 8, the first strain is a compressive strain (see col. 7, lines 20-24).

Regarding to claim 9, the second semiconductor consists essentially of silicon germanium having a germanium content of at least one percent (see col. 4, lines 1-5).

Regarding to claim 10, each of the PFET and the NFET further comprise a layer of silicide contacting gate conductors, source regions and drain regions of the PFET and NFET (see figure 3i-3h, col. 5, lines 30-42).

Regarding to claim 11, the silicide consists essentially of a silicide of cobalt (col. 5, lines 30-42).

Claims 1-7, 9, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharyya (U.S. Publication No. 2004/0065927).

Referring to figures 10-12, Bhattacharyya teaches an integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) (see paragraph# 75) and an n-type field effect transistor (NFET) (see paragraph# 75) wherein a first strain is applied to the channel region of the PFET but not the NFET via a semiconductor layer disposed in source and drain regions of the PFET (74) and not the NFET (see abstract and paragraph# 75), the semiconductor layer being lattice-mismatched to a single-crystal semiconductor disposed in the channel regions of the PFET and NFET (see abstract and paragraph# 76. Noted that silicon germanium or silicon (40) has a lattice-mismatched).

Regarding to claim 2, the channel regions of the PFET and the NFET are disposed in a single crystal region of the first semiconductor (74) and the lattice-mismatched semiconductor includes a layer of a second semiconductor (40) disposed over the single-crystal region of the first semiconductor (see figure 10 and paragraph# 76).

Regarding to claim 3, the single crystal region of the first semiconductor has a main surface defined by a level of a gate dielectric of a gate stack of the PFET (70, see figure 10) and the layer of the second semiconductor has a top surface disposed beneath and main surface (74, see figure 10).

Regarding to claim 4, single-crystal layer of the first semiconductor (40) disposed over of the second semiconductor (74, see figure 10).

Regarding to claim 5, the first semiconductor consists essentially of a semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide (see paragraph# 76) and the second semiconductor consists essentially of another semiconductor different from the first semiconductor, the another semiconductor

selected from the group consisting of silicon, silicon germanium and silicon carbide (see paragraph# 76. noted if the first semiconductor is silicon, the second semiconductor silicon germanium).

Regarding to claim 6, the first semiconductor consists essentially of silicon and the second semiconductor consists essentially of silicon germanium (see paragraph # 76).

Regarding claim 7, the first semiconductor consists essentially of silicon germanium according to a first formula $Si_{x1}Ge_{y1}$, where x1 and y1 are percentages, x1 + y1 = 100%, y1 being at least one percent and the second semiconductor consists essentially of silicon germanium according to a second formula $Si_{x2}Ge_{y2}$, where x2 and y2 are percentages x2 + y2 = 100%, y2 being at least one percent, wherein x1 is not equal to x2 and y1 is not equal to y2 (see paragraph# 80-81, 90-93, wherein the semiconductor is SiGe where Ge is about 10-60%, it means that Si is about 40-90% since silicon and germanium are the only 2 elements that mention in forming the semiconductor layer).

Regarding to claim 9, the second semiconductor consists essentially of silicon germanium having a germanium content of at least one percent (see paragraph# 80-81).

Regarding to claim 12, an integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) (see paragraph# 75) and an n-type field effect transistor (NFET) (see paragraph# 75) wherein a first strain is applied to the channel region of the PFET but not the NFET via a semiconductor layer disposed in source and drain regions of the PFET (74) and not the NFET (see abstract and paragraph# 75), the semiconductor layer being lattice-mismatched to a single-crystal semiconductor disposed in the channel regions of the PFET and NFET (see abstract and paragraph# 76. Noted that silicon germanium or

silicon (40) has a lattice-mismatched) consisting essentially of silicon germanium disposed in source and drain regions of the PFET and not of the NFET (see paragraph# 76), the silicon germanium having proportions according to the formula Si_xGe_y where x and y are percentages each being at least one percent, x plus y equaling 100 percent (see paragraph# 80-81, 90-93, wherein the semiconductor is SiGe where Ge is about 10-60%, it means that Si is about 40-90% since silicon and germanium are the only 2 elements that mention in forming the semiconductor layer).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharyya (U.S. Publication No. 2004/0065927) as applied to claims 1-7, 9, 12 above in view of Xiang (U.S. Patent No. 6,703,648).

Bhattacharyya teaches all of the limitation as described in the claimed invention above. However, the reference does not teach the compressive strain, the cobalt silicide contacting gate conductors, source region and drain regions of the PFET and NFET.

Referring to figures 3a-3i, Xiang et al. teaches:

Regarding to claim 8, the first strain is a compressive strain (see col. 7, lines 20-24).

Regarding to claim 10, each of the PFET and the NFET further comprise a layer of silicide contacting gate conductors, source regions and drain regions of the PFET and NFET (see figure 3i-3h, col. 5, lines 30-42).

Regarding to claim 11, the silicide consists essentially of a silicide of cobalt (col. 5, lines 30-42).

Therefore it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a compressive strain in the semiconductor layer, the cobalt silicide contacting gate conductors, source region and drain regions of the PFET and NFET in process of Bhattacharyya as taught by Xiang et al. because the process would improve hole mobility.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the concentration of silicon and germanium within the semiconductor, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.-silicon/germanium material), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- wherein silicon germanium is equal to 100%) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN